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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,969	02/26/2004	Mu-Tsang Lin	67,200-1230	9427

7590 02/09/2005
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EXAMINER

ORTIZ RODRIGUEZ, CARLOS R

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/789,969	Applicant(s) LIN ET AL.	
	Examiner Carlos Ortiz-Rodriguez	Art Unit 2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 13 rejected under 35 U.S.C. 102(b) as being anticipated by Tam et al. U.S Patent No. 4,507,078.

Regarding claim 13 Tam et al. discloses a method of sensing a position of a wafer on a bake plate, comprising: setting said bake plate at a temperature set point for a baking process; placing said wafer on said bake plate; measuring a change in temperature of said bake plate over a specified time interval; determining whether said wafer is properly positioned on said bake plate based on said change in temperature over said specified time interval; and aborting said baking process in the event that said wafer is improperly positioned on said bake plate (C2 L55-68, C6 L30-36 and C6 L50-62).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-12 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colelli, Jr. et al. U.S Patent No. 6,100,506 in view of Tam et al. U.S. Patent No. 4,507,078.

Regarding claims 1-4, 7-9, and 11 Colelli, Jr. et al. discloses a temperature-sensing wafer position detection system, comprising: a bake plate having a temperature-sensing apparatus operably engaging said bake plate for monitoring a change in temperature of said bake plate upon placement of a wafer on said bake plate (Abstract L10-15 and Fig 1); a controller operably connected to said bake plate for operating said bake plate (Fig 1 element 12 and C2 L60-67).

But Colelli, Jr. et al. fails to clearly specify a microprocessor operably connected to said temperature-sensing apparatus for receiving a temperature data signal from said temperature-sensing apparatus, said microprocessor operably connected to said controller for aborting operation of said bake plate through said controller when said change in temperature of said bake plate falls below a threshold value in a specified time interval.

However, Colelli, Jr. et al in combination with Tam et al. discloses a microprocessor operably connected to said temperature-sensing apparatus for receiving a temperature data signal from said temperature-sensing apparatus, said microprocessor operably connected to said controller for aborting operation of said bake plate through said controller when said change in temperature of said bake plate falls below a threshold value in a specified time interval (see Tam et al. C2 L55-68, C6 L30-36 and C6 L50-62).

Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the above invention suggested by Colelli, Jr. et al. and

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combining it with the invention disclosed by Tam et al. The results of this combination would lead to temperature-sensing wafer position detection system and method.

One of ordinary skill in the art would have been motivated to do this modification because it is known in this art to control a bake plate utilizing temperature and time conditions as suggested by Tam et al.

Regarding claims 5 and 10, Colelli, Jr. et al in combination with Tam et al. further disclose that said bake plate comprises a plate body having a heating surface and a base carried by said heating surface for supporting the wafer in spaced-apart relationship to said heating surface (see Colelli, Jr. et al. C4 L51-53).

Regarding claims 6 and 12, Colelli, Jr. et al in combination with Tam et al. further disclose a wafer guide carried by said base for guiding the wafer onto said base (see Colelli, Jr. et al. C4 L51-53).

Regarding claims 14 and 17-18, Tam et al. discloses all the limitations of the base claims.

But Tam et al. fails to clearly disclose determining whether said wafer is properly positioned on said bake plate comprises determining that said wafer is properly positioned on said bake plate when said change in temperature is at least as great as a threshold value for said change in temperature over said specified time interval.

However, Tam et al. in combination with Colelli, Jr et al. disclose determining whether said wafer is properly positioned on said bake plate comprises determining that said wafer is

properly positioned on said bake plate when said change in temperature is at least as great as a threshold value for said change in temperature over said specified time interval (see Colelli, Jr. et al. C2 L55-68, C6 L30-36 and C6 L50-62).

Regarding claims 15-16 and 19-20, wherein said threshold value is one percent of said set point temperature and wherein said specified time interval is 10 seconds are options of the designer according to the art of record.

Citation of Pertinent Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to temperature-sensing wafer position detection system and method:

- a. U.S. Pat. No. 6,133,550 to Griffiths et al., which discloses method and apparatus for thermal processing of semiconductor substrates.
- b. U.S. Pat. No. 6,355,909 to Griffiths et al., which discloses method and apparatus for thermal processing of semiconductor substrates.
- c. U.S. Pat. No. 6,596,973 to Donald et al., which discloses pyrometer calibrated wafer temperature estimator.

The following publications are cited to further show the state of the art with respect to temperature-sensing wafer position detection system and method:

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g. U.S. Pub. No. 2004/0047993 to Kumar et al., which discloses thermal processing system and methods for forming low-k dielectric films suitable for incorporation into microelectronic devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Ortiz-Rodriguez whose telephone number is (571) 272-3747. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The central official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (703)308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

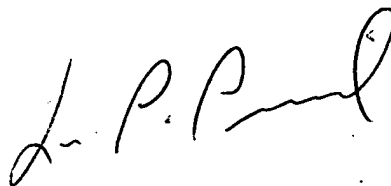
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Carlos Ortiz-Rodriguez
Patent Examiner
Art Unit 2125

cror

February 6, 2005

A handwritten signature in black ink, appearing to read "L. P. Picard". The signature is fluid and cursive, with a large loop at the end.

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100